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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,395	12/12/2003	Hajime Washio	1035-484	9130

23117 7590 10/31/2006

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,395	WASHIO ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 10-12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

Page 1, 2nd paragraph, line 5 the word "*interesting*" should be changed to "**intersecting**."

Page 9, line 6 states: "...*to other circuit than*..." which should be changed to "...**to a circuit other than**..."

DETAILED ACTION

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Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-5 and 7-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Figures 10-12 and page 2, line 1 to page 8, lines 8.) in view of Kazunari (JP 11-031747).

Regarding claim 1, APA discloses a display device (Figure 10), comprising:

a scanning signal line driving circuit for driving scanning signal lines (Figure 10 shows gate driver GD which drives the gate lines GL(1)-GL(n).); and

a data signal line driving circuit for driving data signal lines intersecting the scanning signal lines (Figure 10 shows signal driver SD which drives the signal lines SL(1)-SL(n).),

at least one of a scanning signal line driving circuit and a data signal line driving circuit being supplied with at least first and second signals (Figure 11 and page 6, lines 4-18 explain that signals ck1 and ck2 are both supplied to the first data line driver circuit SD1.),

the first signal being supplied in parallel to other circuit than the driving circuit supplied with the first and second signals (Figure 11 shows that the signal ck1 is supplied also to the second signal driver SD2.), the other circuit being one of the scanning signal line driving circuit, the data signal line driving circuit, and a pre-charging circuit for carrying out pre-charging of the data signal lines (Figure 11 shows that the other circuit is a data driver SD2.),

APA fails to teach the display device further comprising wiring load adjustment section for equalizing wiring load of the second signal which is supplied to the driving circuit, and wiring load of the first signal which is supplied in parallel to the driving circuit and the other circuit.

Kazunari discloses of a display device comprising a wiring load adjustment section for equaling the wiring load of two signals in which the wirings are of different length (Figure 4 and paragraph [0030] explain that wiring 316 has a partial wiring

connected to it, which has a capacitance of 316-A, allowing for the load capacitances of the wirings to be equal.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the teachings of Kazunari with the teachings of APA in order to reduce a difference in delay of the clocks.

Regarding claim 2, this claim is rejected under the same rationale as claim 1.

Regarding claim 3, please refer to the rejection of claim 1.

Regarding claim 4, APA and Kazunari disclose the display device as set forth in claim 2.

APA also discloses wherein the first signal is supplied to the driving circuit and the other circuit from a common input terminal and through a common signal line (Figure 11 shows that the signal ck1 is supplied to the two driving circuits SD1 and SD2 from a common input ck1 and is supplied to both circuits using the same signal line.).

Regarding claim 5, APA and Kazunari disclose the display device as set forth in claim 2.

APA also discloses wherein the first and second signals are clock signals of plural systems, respectively (Figure 11 shows that the signals ck1 and ck2 are clock signals.).

Regarding claim 7, APA and Kazunari disclose the display device as set forth in claim 2.

Kazunari also discloses wherein the wiring load adjustment section adjusts time constants of the respective wirings of the first and second signals (Figure 4 and paragraph [0030]. The examiner interprets that since the partial wiring is added in order to equalize a delay of the different clock signals, then the time constants are being adjusted.).

Regarding claim 8, APA and Kazunari disclose the display device as set forth in claim 2.

APA also discloses wherein the scanning signal lines and the data signal lines are formed on a substrate, and a liquid crystal layer is held between the substrate and a substrate having a counter electrode (Figure 10 shows the gate and signal lines which would be formed on a substrate and liquid crystal would be held between two substrates with the other substrate having a counter electrode as is well known in LCDs.).

Kazunari also discloses that the wiring load adjustment section is constituted of dummy wiring connected to the wiring of a signal (Figure 4 and paragraph [0030] explain that wiring 316 has a partial wiring connected to it, which has a capacitance of 316-A, allowing for the load capacitances of the wirings to be equal.). Therefore based on the combination of references, if the dummy wiring taught by Kazunari is used with

the device taught by APA, the dummy wiring would be connected to the wiring of the second signal which is supplied to the driving circuit.

Regarding claim 9, APA and Kazunari disclose the display device as set forth in claim 8.

APA and Kazunari fail to explicitly teach wherein the dummy wiring is formed in a fanfold shape on a vacant area, which is an area holding the liquid crystal layer on the substrate having a counter electrode, and being provided as a part of a display section but is not involved in image display, the vacant area being closer to an end portion of the substrate than the data signal line driving circuit, however, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to create the wiring in a area in which no other part of the circuit is formed in order to save space and not cause undue increase in circuit size.

Regarding claim 10, APA and Kazunari disclose the display device as set forth in claim 8.

APA and Kazunari fail to explicitly teach wherein the dummy wiring is formed in a plate shape to be in parallel with the counter electrode, however, to create the dummy wiring in a specific shape and form would have been a matter of design choice.

Regarding claim 11, APA and Kazunari disclose the display device as set forth in claim 8.

APA and Kazunari fail to explicitly teach wherein the dummy wiring is formed in a periphery of a display section involved in image display, however, to create the dummy wiring in a specific location of the circuit would have been a matter of design choice.

Regarding claim 12, APA and Kazunari disclose the display device as set forth in claim 2.

APA also disclose wherein the scanning signal lines and the data signal lines are formed on a substrate where an interlayer insulation film and a conductive film are formed (Figure 10 shows the gate and signal lines which would be formed on a substrate and it is well known that an interlayer insulation film and a conductive film are provided on the substrate with the gate and signal lines.).

Kazunari also discloses that the wiring load adjustment section is constituted of dummy wiring connected to the wiring of a signal (Figure 4 and paragraph [0030] explain that wiring 316 has a partial wiring connected to it, which has a capacitance of 316-A, allowing for the load capacitances of the wirings to be equal.). Therefore based on the combination of references, if the dummy wiring taught by Kazunari is used with the device taught by APA, the dummy wiring would be connected to the wiring of the second signal which is supplied to the driving circuit.

Regarding claim 13, this claim is rejected under the same rationale as claim 11.

Regarding claim 14, APA and Kazunari disclose the display device as set forth in claim 2.

APA also discloses wherein the scanning signal lines and the data signal lines have a thin film transistor for each intersection (Figure 10 shows the gate and signal lines which have a pixel circuit at the intersection, which would contain a TFT.).

Kazunari also discloses that the wiring load adjustment section is constituted of dummy wiring connected to the wiring of a signal (Figure 4 and paragraph [0030] explain that wiring 316 has a partial wiring connected to it, which has a capacitance of 316-A, allowing for the load capacitances of the wirings to be equal.). Therefore based on the combination of references, if the dummy wiring taught by Kazunari is used with the device taught by APA, the dummy wiring would be connected to the wiring of the second signal which is supplied to the driving circuit.

Regarding claim 15, this claim is rejected under the same rationale as claim 11.

Regarding claim 16, APA and Kazunari disclose the display device as set forth in claim 2.

APA and Kazunari fail to teach wherein the other circuit is a pre-charging circuit for carrying out pre-charging of the data signal lines, however, it is well known that liquid crystal device can contain a pre-charging circuit for pre-charging the data signal lines.

Regarding claim 17, APA and Kazunari disclose the display device as set forth in claim 2.

APA and Kazunari fail to teach wherein the wiring load adjustment section is provided in the scanning signal line driving circuit, however, to place the wiring load adjustment section in a specific location of the circuit would have been a matter of design choice.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Figures 10-12 and page 2, line 1 to page 8, lines 8.) in view of Kazunari (JP 11-031747) and further in view of Kim (US 5,808,596).

Regarding claim 6, APA and Kazunari disclose the display device as set forth in claim 2.

APA and Kazunari fail to teach wherein the signals are digital image signals constituted of a plurality of bits, and are divided into at least two bit groups.

Kim discloses wherein signals are digital image signals constituted of a plurality of bits, and are divided into at least two bit groups (Figure 2 and column 3, lines 40-57 explain that the signals (b) and (c) are pixel data, i.e. image signals, where it is well know that pixel data can be in digital form constituted of a plurality of bits being divided into at least two bit groups.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the idea of compensating for delay of image signals

as taught by Kim with the display device taught by the combination of APA and Kazunari in order to create a high resolution liquid crystal display which does not require excessive increases in clock frequency in order o increase resolution.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ootake et al. (US 2003/0038664) disclose of making the wiring lengths and the wiring capacitances of input wirings and the wiring lengths and the wiring capacitances of the output wirings such that the noise caused by the crosstalk will not affect the adjacent wirings, and the skews between the clock signals and the jitters of respective clock signals can be eliminated.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

25 October 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER